ATTORNEY'S DOCKET NO.: S1022.81042US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jean-Michel MOREAU
Serial No.: 10/812,843
Filed: March 30, 2004
For: CRT VERTICAL SCANNING CIRCUIT WITH A LOW RANGE POWER STANDBY

Examiner: Unassigned
Art Unit: 2821 Confirmation No. 3125

Office of Public Records
Commissioner for Patents
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Sir/Madam:

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[X] Request for corrected publication
[X] Copies of: Pp 8-9 of the Apl. as Filed, Fig. 4 and P 3 of Pub Apl. No. 2004/0257008 A
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Gail Driscoll

Attorney Docket No.: S1022.81042US01
X02/23/05

Respectfully submitted,

Jean-Michel Moreau, Applicant

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REQUEST FOR CORRECTED PUBLICATION PURSUANT TO 37 CFR 1.221(b)

Sir/Madam:

Applicant respectfully requests correction of a material mistake, made in published patent application No. 2004-0257008 A1, published on December 23, 2004.

Specifically, Applicant notes that on page 3, paragraph [0043], line 51, of published patent application No. 2004-0257008, reference indicator "C5" has been replaced with "CS". This is incorrect. All of the collectors in the instant application are identified with a "C". To differentiate one collector from another, as they vary in size, each collector is further identified by a number, such as C5, C6, C7. No collector is identified with a reference indicator using two letters, such as CA, CB, etc.

Identifying the largest zone of two unequal areas as being collector "CS" could be quite confusing as one would not associate collector CS, in the published specification with collector C5 elsewhere in the specification and in Fig. 4. There is no other reference to the collector "CS" anywhere in the specification or in the drawings while references to collector C5 can be found through out the two paragraphs beginning on page 8, line 30 through page 9, line 16. To substitute the reference indicator "CS" for the reference indicator "C5" makes no sense as the collectors are identified numerically not alphabetically.

Applicant wishes to make this correction to the published application and, for the convenience of the Examiner, encloses herewith highlighted copies of pages 8 and 9 of the application as filed, Fig. 4 and Page 3 of published patent application No. 2004/0257008 A1, highlighting the corresponding text as it appears in the publication

Should any questions arise concerning the foregoing, the Examiner is invited to call the undersigned at the number listed below.

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transistor T6. Consequently, the output of comparator 12 is low and no current is provided by the reference current source Iref.

In standby mode, the voltage between the collector and the emitter of transistor T6 decreases and transistor T6 goes to saturation. The voltage between terminal Tup and the collector of transistor T6 is lower than the voltage of the reference supply source 13. The output of comparator 12 is high, and a reference current is provided to transistor T3. Thus, the current through transistor T3 is higher than the current through transistor T4. Consequently, the voltage of control signal c is low and the output of power amplifier 4 is biased towards the voltage of terminal Tup. The power consumption is minimal.

Figure 3 is a top view of transistor T6 of the differential amplifier 3 together with added elements forming an embodiment of the present invention. P-type zones are hatched and N-type zones are white. In this example, the emitter is a small circular P-type zone 20. The emitter is surrounded by a circular N-type zone 21 forming the base of the transistor. The base is surrounded by a P-type zone 22 forming the collector of the transistor. The external outline of the collector forms a square. A P-type zone 23 forming an auxiliary collector is near the right side of the collector of the transistor, both collectors being separated by a very small N-type zone 24. The auxiliary collector is connected to the collector of transistor T3.

In standby mode, the transistor T6 is saturated as described previously. Electrical carriers are injected from the collector of transistor T6 to the auxiliary collector. An auxiliary current is created in the auxiliary collector. The auxiliary current provided to transistor T3 unbalances the pair of transistors T3-T4 and the control signal c is low.

During normal operation, the transistor T6 is not saturated and no auxiliary current is provided, the differential amplifier operates normally.

By adding an auxiliary collector zone having a very small area compared to the global area of the differential amplifier 3, it is possible to obtain the result sought for, i.e. to have a power consumption always minimal in standby.

Figure 4 is a top view of transistors T5, T6 and T7 of the differential amplifier 3 of figure 2 according to another embodiment of the present invention. P-type zones

are also hatched and N-type zones are white. The emitter common to all transistors is a small circular P-type zone 30. The emitter is surrounded by a circular N-type zone 31 forming the common base of all transistors. All collectors are realized within a rectangular shaped zone surrounding the base. The bottom half part of the rectangular shape constitutes the collector C6 of transistor T6. The top half part of the rectangular shape zone is divided into two unequal area zones, the smaller zone being the collector C7 of transistor T7, the largest zone being the collector C5 of transistor T5. Collectors C5, C6 and C7 are separated by narrow N-type zones. Though collectors C5 and C7 have different areas, the length of the outline of C7 opposite to the outline of the emitter is equal to the length of the outline of C5 opposite to the outline of the emitter. However, the length of the outline of C5 opposite to the outline of C6 is larger than the length of the outline of C7 opposite to the outline of C6.

In standby mode, electrical carriers are emitted by collector C6 and injected into collectors C5 and C7. As the opposite outline lengths between collectors C5/C6 and collectors C7/C6 are different, the current created in collector C5 is higher than the current created in collector C7.

Figure 5 is an equivalent circuit of the differential amplifier 3 implemented with transistors T5, T6 and T7 realized as described previously in relation to figure 4. In fact, two transistors T9 and T10 are added to the differential amplifier 3. The collector of transistor T8 is connected to the base of transistors T9 and T10. The emitters of transistors T9 and T10 are connected to the collector of transistor T6. The sizes of transistors T9 and T10 are different, T9 being larger than T10. The collector of transistor T9 is connected to the collector of transistor T3. The collector of transistor T10 is connected to the collector of transistor T4.

During normal operation, transistor T6 is not saturated and the voltage of its collector is lower than the voltage of its base. Thus, the transistors T9 and T10 are off.

In standby mode, the collector voltage of transistor T6 is higher than its base voltage. The transistors T9 and T10 are on. As transistor T9 is larger than transistor T10, the current provided to transistor T3 is higher than the current provided to transistor T4. Thus, the control signal c is low and the power consumption is minimal.

through transistor T2. Consequently, the voltage on the emitter of transistor T3 is higher than the voltage on the emitter of transistor T4. As a result, the voltage difference between the base and the emitter of transistor T4 is higher than the voltage difference between the base and the emitter of transistor T3. The currents delivered to transistors T3 and T4 are equal, as they are imposed by the current mirror constituted of transistors T5, T6 and T8. As a result, the current drawn by transistor T4 is higher than the current provided by transistor T7. As a consequence, the control signal c decreases. More precisely, the control signal c is lower than a common mode voltage V_{cm} which corresponds to the voltage of control signal c when input signals E^- and E^+ are equal and the current through the deflection coil Ly goes from terminal Tup to the ground through "high-side" current paths of the power amplifier **4**.

[0033] Conversely, when the voltage of negative input signal E− is higher than the voltage of positive input signal E+, the control signal c is higher than the common mode voltage V_{cm}.

[0034] In standby mode, the voltage of terminal Tup is around zero as it is linked to the ground by the diodes **7** as described previously. The input signals E^- and E^+ are around zero. As a consequence, the transistors T1 and T2 are both off. The currents through transistors T3 and T4 are equal and fixed by transistors T5 and T7. As the matching of transistors T3 and T4, resistors R1 and R2 and transistors T5 and T7 cannot be perfect, the control signal c cannot be predicted, and differs from a chip to another. If resistor R2 is a little larger than resistor R1, or if transistor T3 is larger than transistor T4, or if transistor T7 is larger than transistor T5, the control signal c is high, near the ground in this case. Conversely, if resistor R1 is larger than resistor R2, or if transistor T4 is larger than transistor T3, or if transistor T5 is larger than transistor T7, the control signal c is low, near the voltage of Tdown.

[0035] According to the present invention, a circuit **11** is provided to make sure that the control signal c is always low in standby mode, so that the above-mentioned low-side current paths are never activated in standby mode.

[0036] In circuit **11**, a comparator **12** receives on its negative input a fixed voltage equal to the voltage of terminal Tup minus the voltage of a reference supply source **13**. The positive input of comparator 12 is connected to the collector of transistor T6. A reference current source Iref, controlled by comparator **12**, is connected to the collector of transistor T3.

[0037] During normal operation, when terminal Tup is powered, the transistor T6 is in active mode. The voltage of the collector of transistor T6 depends on the voltage of input signals E− and E+ produced by circuit **6**, it is usually in the range 0-4 V when the voltage of terminal Tup is equal to +12 V. The voltage of the reference supply source **13** is chosen lower than the voltage between terminal Tup and the collector of transistor T6. Consequently, the output of comparator **12** is low and no current is provided by the reference current source Iref.

[0038] In standby mode, the voltage between the collector and the emitter of transistor T6 decreases and transistor T6 goes to saturation. The voltage between terminal Tup and the collector of transistor T6 is lower than the voltage of the reference supply source **13**. The output of comparator **12** is high, and a reference current is provided to transistor T3. Thus, the current through transistor T3 is higher than the current through transistor T4. Consequently, the voltage of control signal c is low and the output of power amplifier **4** is biased towards the voltage of terminal Tup. The power consumption is minimal.

[0039] **FIG. 3** is a top view of transistor T6 of the differential amplifier **3** together with added elements forming an embodiment of the present invention. P-type zones are hatched and N-type zones are white. In this example, the emitter is a small circular P-type zone **20**. The emitter is surrounded by a circular N-type zone **21** forming the base of the transistor. The base is surrounded by a P-type zone **22** forming the collector of the transistor. The external outline of the collector forms a square. A P-type zone **23** forming an auxiliary collector is near the right side of the collector of the transistor, both collectors being separated by a very small N-type zone **24**. The auxiliary collector is connected to the collector of transistor T3.

[0040] In standby mode, the transistor T6 is saturated as described previously. Electrical carriers are injected from the collector of transistor T6 to the auxiliary collector. An auxiliary current is created in the auxiliary collector. The auxiliary current provided to transistor T3 unbalances the pair of transistors T3-T4 and the control signal c is low.

[0041] During normal operation, the transistor T6 is not saturated and no auxiliary current is provided, the differential amplifier operates normally.

[0042] By adding an auxiliary collector zone having a very small area compared to the global area of the differential amplifier **3**, it is possible to obtain the result sought for, i.e. to have a power consumption always minimal in standby.

[0043] **FIG. 4** is a top view of transistors T5, T6 and T7 of the differential amplifier 3 of **FIG. 2** according to another embodiment of the present invention. P-type zones are also hatched and N-type zones are white. The emitter common to all transistors is a small circular P-type zone **30**. The emitter is surrounded by a circular N-type zone **31** forming the common base of all transistors. All collectors are realized within a rectangular shaped zone surrounding the base. The bottom half part of the rectangular shape constitutes the collector C6 of transistor T6. The top half part of the rectangular shape zone is divided into two unequal area zones, the smaller zone being the collector C7 of transistor T7, the largest zone being the collector CS of transistor T5. Collectors C5, C6 and C7 are separated by narrow N-type zones. Though collectors C5 and C7 have different areas, the length of the outline of C7 opposite to the outline of the emitter is equal to the length of the outline of C5 opposite to the outline of the emitter. However, the length of the outline of C5 opposite to the outline of C6 is larger than the length of the outline of C7 opposite to the outline of C6.

[0044] In standby mode, electrical carriers are emitted by collector C6 and injected into collectors C5 and C7. As the opposite outline lengths between collectors C5/C6 and collectors C7/C6 are different, the current created in collector C5 is higher than the current created in collector C7.

[0045] **FIG. 5** is an equivalent circuit of the differential amplifier **3** implemented with transistors T5, T6 and T7 realized as described previously in relation to **FIG. 4**. In

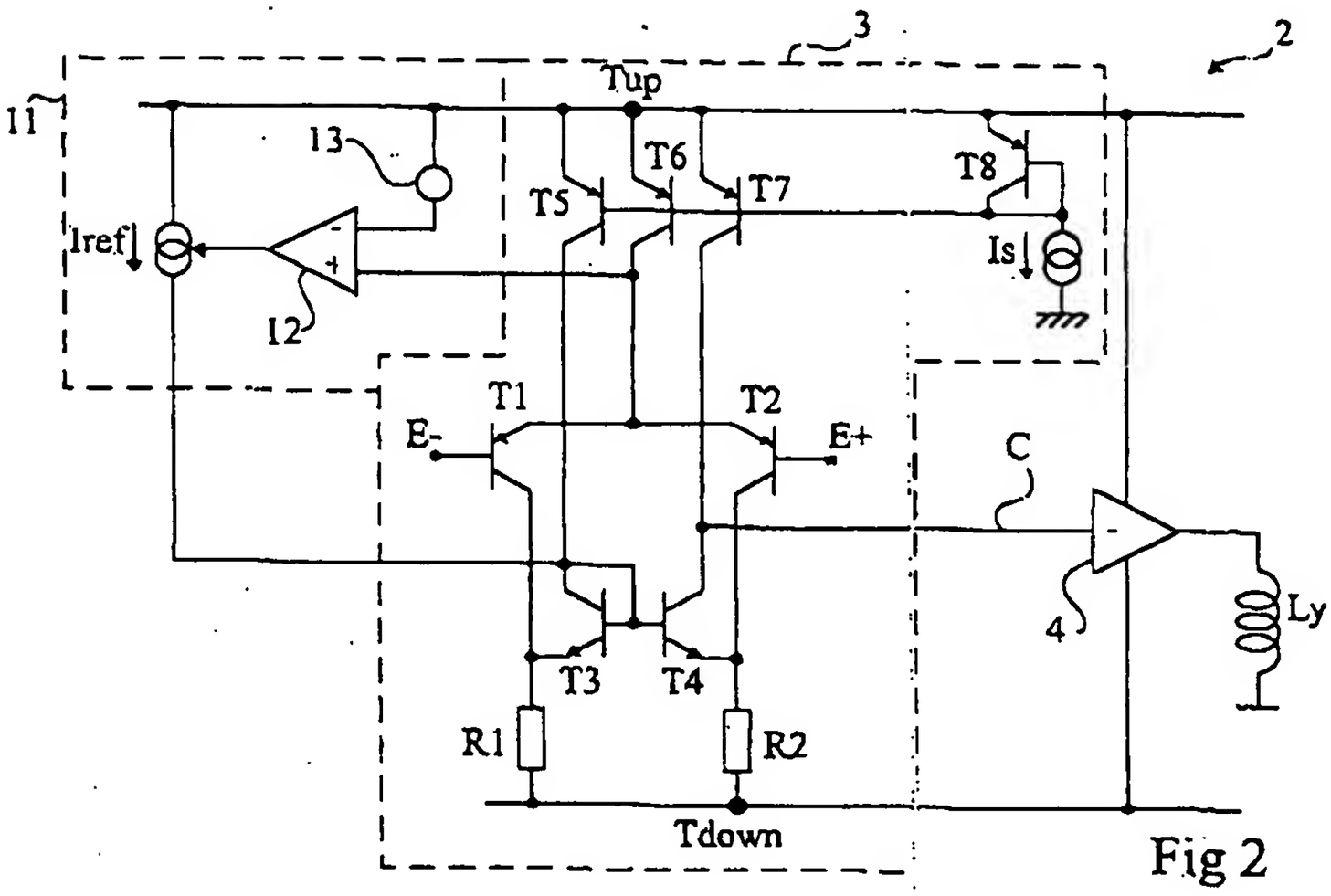

Fig 2

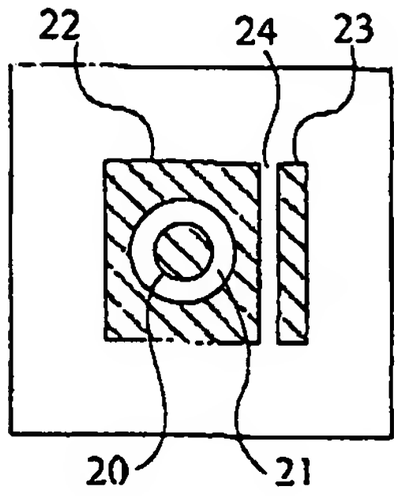

Fig 3

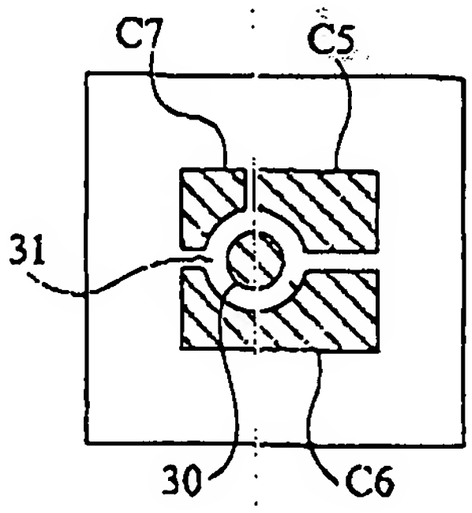

Fig 4

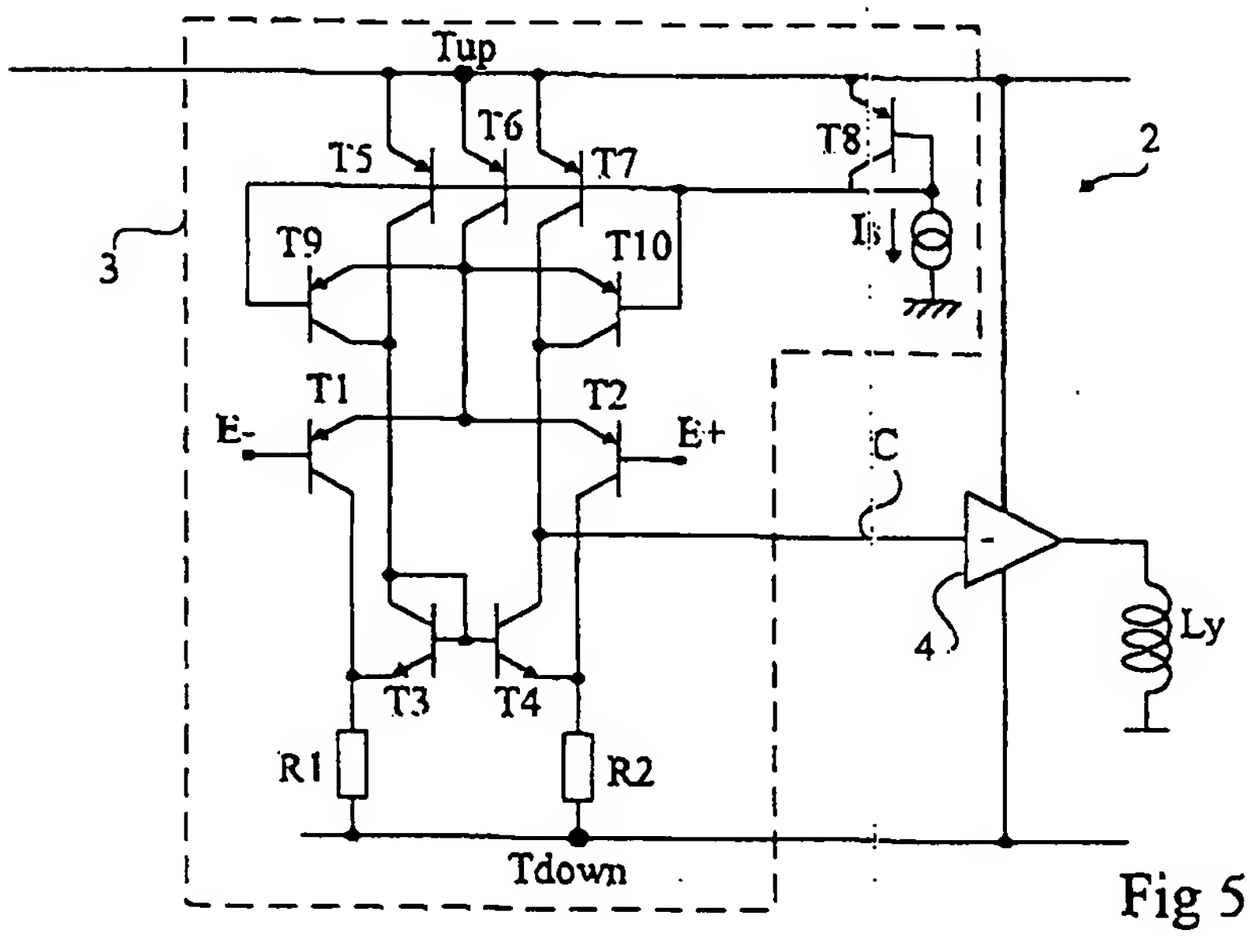

Fig 5